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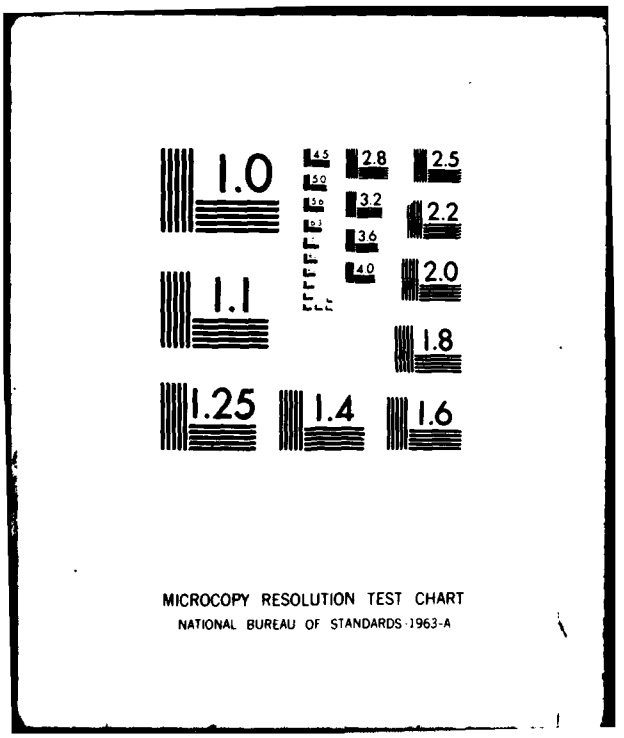
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PRELIMINARY COMPUTER SIZING ESTIMATES FOR AUTOMATED EN ROUTE ATC (AERA)

OCTOBER 1979

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
OFFICE OF SYSTEMS ENGINEERING MANAGEMENT
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16. Abstract

The Federal Aviation Administration is presently analyzing requirements for the computer system that will replace the IBM Model 9020 computers, that currently support the en route NAS system, as well as the computers that support the terminal ARTS facilities. As an early input to the requirements analysis effort, the FAA's Office of System Engineering Management requested a preliminary analysis of computer loads imposed by near-term enhancements to the existing NAS and certain long-term enhancements. This report presents an analysis that estimates the computer sizing requirements imposed by the Automated En Route Air Traffic Control (AERA) system, a possible long-term enhancement to NAS. In order to establish preliminary AERA processor and memory requirements, two models are presented. A simulation model of the higher level AERA functions, such as initial processing and progress monitoring, is applied to the Washington Center to show typical AERA imposed processor loading. A previously developed linear model of required memory is also applied to show typical memory requirements resulting from AERA.

The models presented reflect a version of AERA existing during December, 1978. That version of AERA did not include the recently developed concepts of strategic and tactical planning/control. Additionally, since AERA will continue to evolve during the development stage, requirements enumerated must be considered preliminary in nature and significant changes on the estimates may be expected. Throughout this analysis, it is assumed that there is no integration of the existing NAS functions and the AERA functions. This implies that the requirements presented here cannot be simply added to estimates of NAS requirements.

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CONCLUSIONS

Based on the application of the preliminary simulation model of higher level AERA functions and of the model estimating AERA memory requirements to the Washington Center, the following conclusions have been reached.

1. Figure 1 presents average processor utilization, in terms of IBM 9020A and DEC PDP 11/70 seconds per second, if all AERA functions generated during a given ten second period were processed at the end of the given period. Note that these are average estimates for processing required during each ten second period and, as such, do not account for peak utilization and response time considerations. Relative to processor requirements for the existing NAS (which is believed to require no more than three 9020A seconds per second, for instantaneous aircraft counts (IACs) of less than 250), AERA will impose significant processor requirements.

2. A conservative estimate of AERA imposed memory (buffered and non-buffered) requirements indicated three million bytes of storage could accommodate IACs of over 400. Hence, it appears that the AERA imposed memory requirements will not require technology development beyond currently available memory systems.

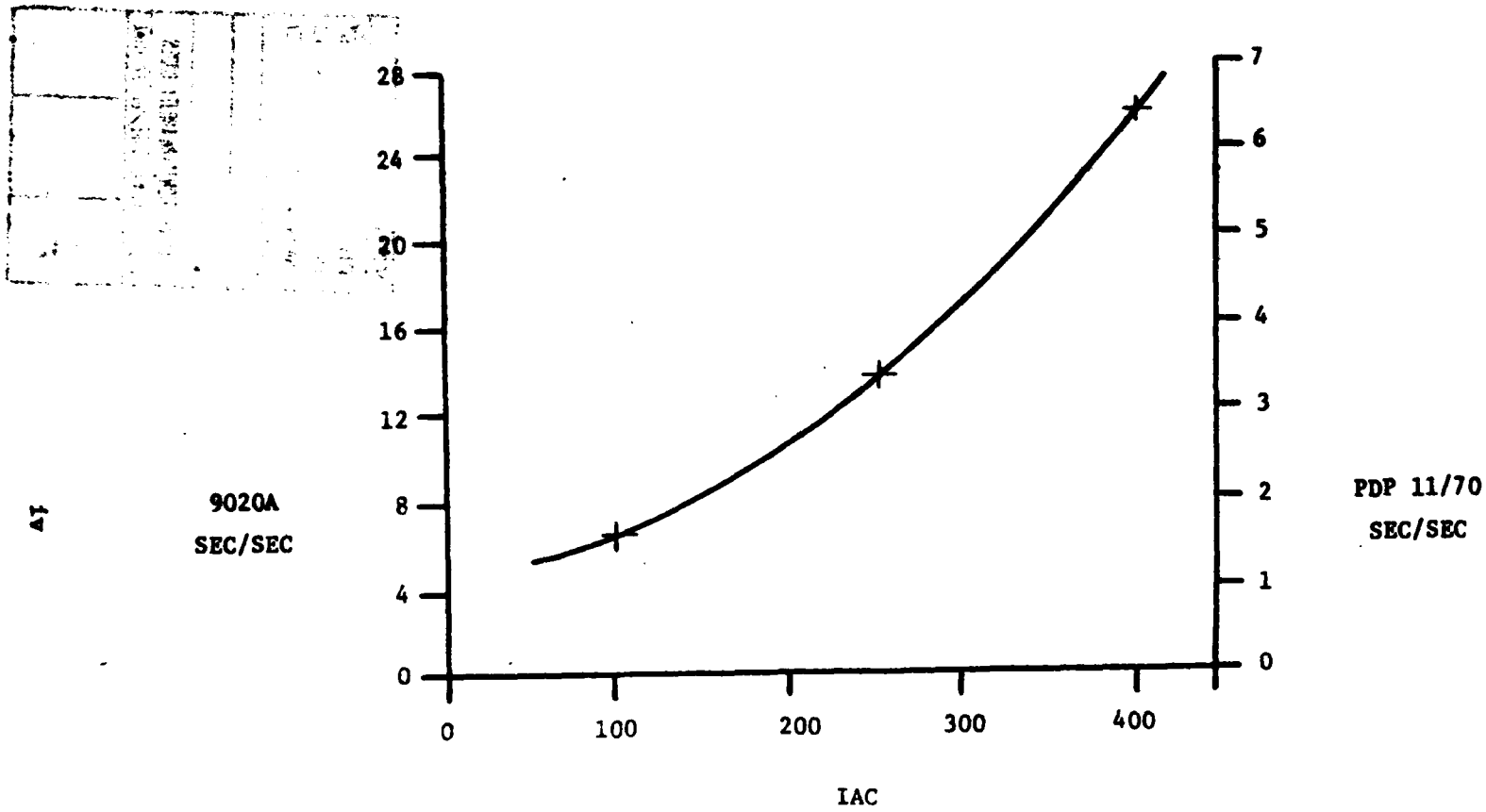

FIGURE 1
AVERAGE UTILIZATION OF TEN SECOND PERIOD
DUE TO AN AERA IMPOSED LOAD

PREFACE

This report presents an analysis of the computer requirements imposed by AERA. In discussing the models developed the author assumes that the reader has a basic understanding of the automation concepts encompassed by AERA. The reader may want to see MTR-79W00167, "Automated En Route ATC (AERA): Operational Concepts, Package 1 Description, and Issues" for an introduction.

The author wishes to thank Mr. Richard W. Telsch of The MITRE Corporation for his contributions to this report. Mr. Telsch had previously developed the memory model presented in the report and supplied considerable background information of the modeled AERA functions.

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1. INTRODUCTION

The Federal Aviation Administration is presently considering the replacement of its ATC computer systems, including the complement of IBM Model 9020 computers which are used to support the present enroute NAS system. As a part of this effort, the Office of Systems Engineering Management is compiling a list of computer requirements imposed by near-term and long-term improvements to the existing system. These improvements, together with the existing NAS functions, comprise a large subset of the functions that will be supported at some time by the replacement system. The primary long-term improvement considered in the requirements compilation is the Automated Enroute Air Traffic Control (AERA) System. The purpose of this report is to establish preliminary estimates of processor and memory requirements that will be imposed by AERA.

The primary tool utilized in this requirements analysis was a functional model of AERA imposed processing load. The functional model is a simulation of the higher level AERA functions (i.e., initial processing and progress monitor) and enables an analysis of the processor loading due to these AERA functions. The modeling approach specifically addresses the dynamics of the higher level functions, but considers the lower level computer functions such as page swapping and input/output waits as part of these higher level functions and does not specifically model them. This simulation model was implemented in GPSS.

Required inputs and background material for the AERA functional model, as well as a previously developed memory sizing model, have been obtained from the AERA development effort. More specifically, the models are based on a simulated version of AERA existing during December, 1978. Hence, the recently developed concepts of strategic and tactical planning/control are not considered in this analysis. It should be noted that AERA is still in early developmental stages and as such the estimates generated in this analysis are preliminary. However, these requirements estimates should be refined to reflect a more complete understanding of AERA as development continues.

The analysis in this report assumes that the computer requirements imposed by AERA are independent of requirements due to NAS and its enhancements. This implies no integration of the AERA and NAS functions. However, due to similarities of various functions, an implemented version of AERA would most likely be integrated into the NAS. This integration would result in the deletion of duplicated functions. The implication to enumeration of requirements is that the AERA requirements presented here cannot be simply added to NAS requirements to obtain a realistic estimate of total requirements without first examining the integration problem. Hence, prior to

a determination of total computer requirements, an examination of the AERA/NAS integration problem and its impact on these AERA models must be made.

As will be discussed, the analysis of AERA imposed processor loading did not assume a specific computer system architecture. Therefore, estimates for functional response time were unable to be made. As computer system architectures are proposed as potential ATC computer replacement systems, the simulation model could be easily revised to model specific architectures and to estimate processor utilization and response time.

There are two additional sections of this report. Section 2 of this report presents an overview of the developed functional model as well as a specification of each individual function. Also presented in Section 2 is a description of a model developed to determine the memory requirement due to AERA. Section 3 presents the results of applying the developed processor loading and memory models. Since these sections document detailed technical analysis, the reader is assumed to have an understanding of the AERA design language and implementation.

2. THE MODELS

2.1 Processor Loading Model

Figure 2-1 presents an overview of the developed functional level model used to assess the processor loading due to AERA. The model is comprised of three basic components: a traffic generator and simulator, which is responsible for simulation of a traffic load through the given center; an AERA function generator, which generates AERA functions (e.g., initial processing, conflict resolution) based on an aircraft flight progress; and a processor simulator, which simulates the performance of a processor architecture given the generated AERA function load. The primary model inputs include ARTCC environment data and data specifying a particular traffic scenario. The model could optionally receive as inputs real traffic data and/or real AERA function data and, hence, not require aircraft simulation or AERA function generation. The model output is a set of performance measures, such as processor utilization. These performance measures will be described in detail in Section 3. A discussion of each model component now follows.

2.1.1 Traffic Generator and Simulator

The traffic generator and simulator generates aircraft and simulates the aircraft's flight through a center. Three classifications of aircraft are generated and simulated: traffic overflying the center (overflights), traffic entering the center and metered for landing at a major hub (arrivals), and traffic having a departure point and arrival point within the center (intra-center). Aircraft departing major hubs within the center are considered as a part of the overflight traffic classification.

Figure 2-2 presents a flow diagram that describes the typical aircraft flight through the center. Aircraft flight is simulated by determining for each aircraft the time at which significant pre-determined events (i.e., center boundary crossing, descent initiation) occur. Aircraft generation in each traffic classification is random. Thus, each aircraft is generated based on an exponentially distributed time between generation, the mean of which is a specified input. After the aircraft is generated, simulation of the flight through the center is begun. If the aircraft is part of the intra-center traffic classification, the flight is initiated (e.g., take-off and climb phases). If the aircraft is an arrival or an overflight, the aircraft is flown to the center boundary. That is, the point at which the aircraft comes under the direct control of the center. Prior to this boundary, the center has knowledge of the aircraft but not control. After reaching the in-bound center boundary, overflights are flown through the

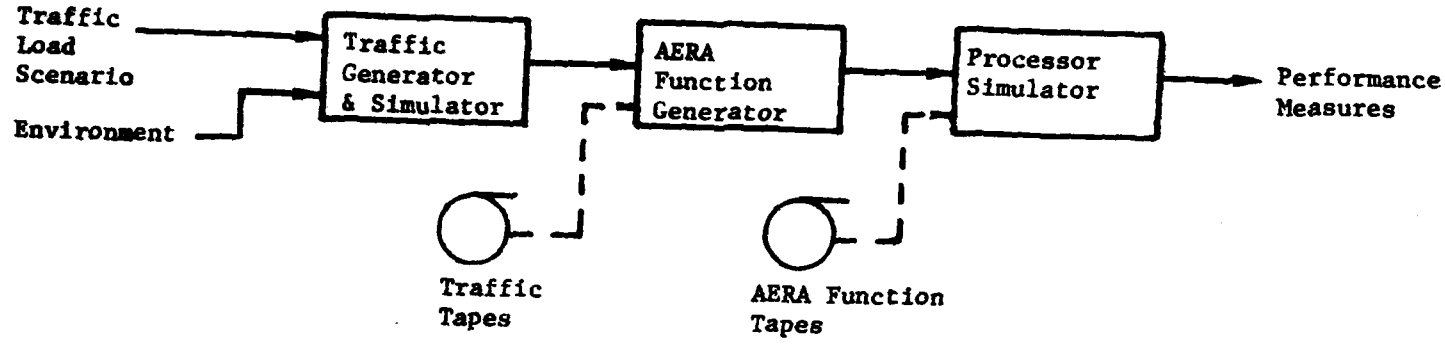

FIGURE 2-1
OVERVIEW OF FUNCTIONAL PROCESSOR LOADING MODEL

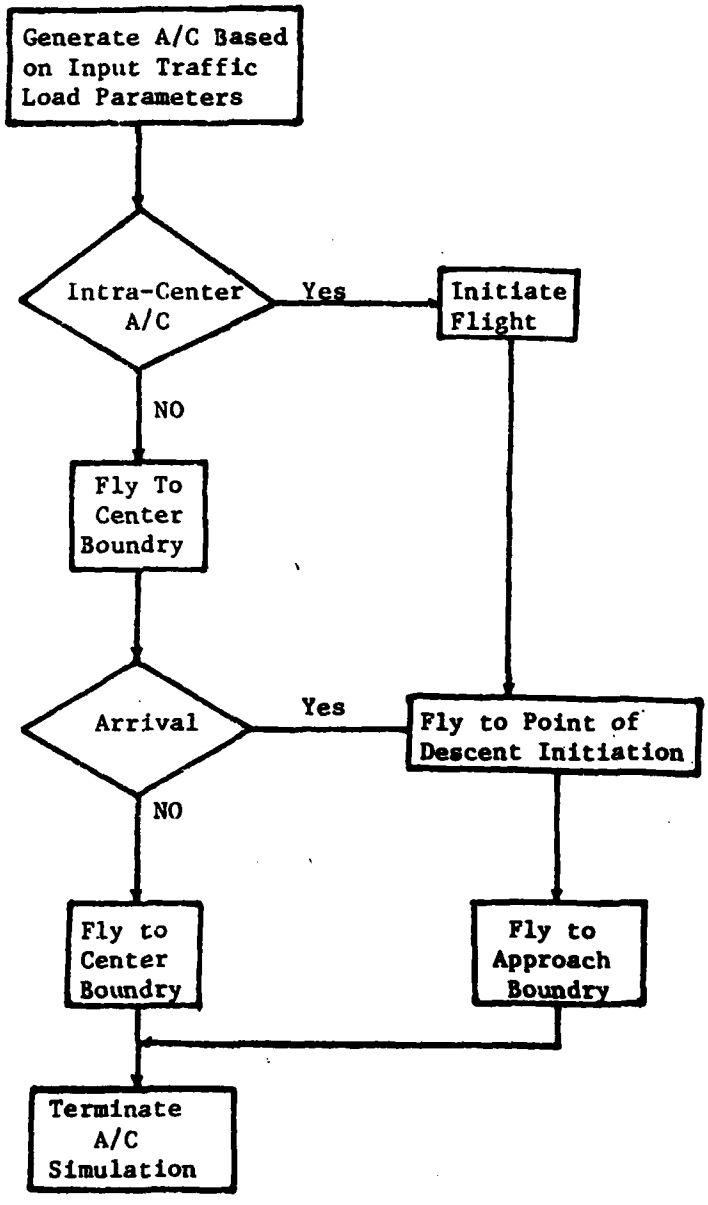

FIGURE 2-2
SIMULATION OF AIRCRAFT FLIGHT THROUGH CENTER

center to the boundary where the aircraft comes under the control of another center. Arrivals and intra-center aircraft are flown to the point at which they begin descending. These aircraft begin their descents and are flown to the approach boundary where they are no longer under the control of the center. The duration of flight time through the center is normally distributed for each traffic classification. The mean and standard deviation are specified as input data for each of the traffic classifications. While this simulation of aircraft flight is very simplistic, it is assumed to be an adequate method of providing pertinent aircraft flight information to the AERA function generator. Flight information is provided by the traffic generator and simulator at various points in the flight profile (e.g., point of descent, crossing of center boundary) or when queried by the AERA function generator.

2.1.2 AERA Function Generator

The AERA function generator is responsible for the generation and definition of AERA functions based on individual aircraft flight progress or on predetermined system requirements. After determining that an AERA function is to be generated, the function generator then determines the associated amount of processing time required. The required processing time for a function varies between invocations of the same functions due to the simulation dynamics (e.g., actual traffic, specific aircraft data). The required processing time is determined by algorithms specified for each of the higher level AERA functions. Basically, the function algorithms determine which tasks, with known deterministic processing times, must be dynamically invoked by the AERA funcion being defined. After the functions are defined, they are queued at the processor simulation for service.

The independent high level AERA functions considered in the model are enumerated in Table 2-1. In the course of defining these functions, the AERA function generator typically determines that the conflict prediction and conflict resolution tasks must be invoked as a part of the AERA function. The prediction and resolution tasks are then defined by specified algorithms in the same manner as the other AERA functions.

Each of the functions are now discussed. Appendix A contains an explanation of the notation utilized.

2.1.2.1 Initial Processing Function

The initial processing function is invoked for each aircraft at the time when the center receives information that the aircraft will soon enter its airspace or come under its control. Relative to the traffic simulator, this event occurs as soon as the aircraft is

TABLE 2-1
INDEPENDENT HIGH LEVEL AERA FUNCTIONS MODELED

TASK	DESCRIPTION
INITIAL PROCESSING	INITIAL STRATEGIC PLANNING OF AIRCRAFT THROUGH CENTER, CONFLICT PREDICTION AND RESOLUTION IF REQUIRED, INSERTION INTO METERING SCHEDULE AND METERING COMMAND GENERATION IF AIRCRAFT IS AN ARRIVAL
PERIODIC UPDATE	UPDATES CONFLICT PREDICTION (PERFORMS RESOLUTION IF REQUIRED), MONITORS METERING PROGRESS. INVOKED FOR EACH AIRCRAFT EVERY FIVE MINUTES
REAL TIME CYCLE OVERHEAD	DISPLAYS, DATA RECORDING, ETC.
PROGRESS MONITOR	DETERMINES IF AIRCRAFT HAVE DEVIATED FROM PLANNED FLIGHT. IF SO, REBUILDS STATE SEGMENTS, CHECKS CONFLICT PREDICTION, PERFORMS CONFLICT RESOLUTION IF NECESSARY. INVOKED EVERY THREE MINUTES FOR ALL AIRCRAFT
CLEARANCE DELIVERY	DELIVERS CLEARANCES TO AIRCRAFT AND UPDATES APPROPRIATE DISPLAYS AS NECESSARY.
HANDOFF MANAGEMENT	CONTROLS THE PROCEDURAL HANDOFF BETWEEN TWO ADJACENT CENTERS
WIND UPDATE	PERIODICALLY UPDATES WIND ESTIMATES.

generated. Figure 2-3 presents the definition of the initial processing function. This algorithmic definition determines the required processing time for each specific invocation of initial processing. The notation t_i represents required processing time due to the use of particular task. The total processing time is the sum of all terms in all blocks of the flow diagram.

The initial processing function begins by requiring processor resources for the overhead in setting up the aircraft bead and for absorbing prior sector data ($t_{ABC} + t_{PSB}$). Then processing time is required to run the flight route follower, build the vertical profile, and build state segments ($t_{FRF} + t_{VPR} + t_{BSS}$). The processing time for these tasks are directly proportional to the aircraft's flight distance through the center (d_C). Processing time for several tasks to update displays and record data ($t_{FPM} + t_{PRM} + t_{DRP}$) is then required. If the aircraft is not an arrival (i.e., overflight or intra-center traffic classification), processing time for conflict prediction (t_{CP}) and conflict resolution (t_{CR}), if necessary, is then required.

If the aircraft is an arrival, processing time is then allowed to insert into the metering schedule (t_{MCG}). The time to process state segment rebuilding (t_{BSS}), conflict prediction (t_{CP}) and conflict resolution (t_{CR}), if necessary, is then determined.

At this point, the initial processing for the subject aircraft is complete. However, there is a probability that other aircraft were affected during the process of inserting the subject aircraft into the metering schedule. For each aircraft affected, a metering command is generated (t_{MCG}), the state segment is rebuilt (t_{BSS}), and conflict prediction and resolution, if required, are invoked.

2.1.2.2 Handoff Management Function

The handoff management function is invoked each time an aircraft crosses a center boundary, and hence, is handed off from or to another control center. Figure 2-4 presents the functional definition. As can be seen, the handoff management function is deterministic and consists of only one term (t_{HOF}).

2.1.2.3 Progress Monitor Function

The progress monitor function is invoked every three minutes by the AERA system for the purpose of monitoring the progress of all aircraft. Figure 2-5 defines the algorithm for deterining required processing time for this function.

Progress monitor starts by requiring processing time for checking each of the active aircraft (n_C) to determine if any have deviated from its projected flight profile (t_{PMM}) and to update the flight plan billboard (t_{FPM}). The term n_C includes all aircraft under

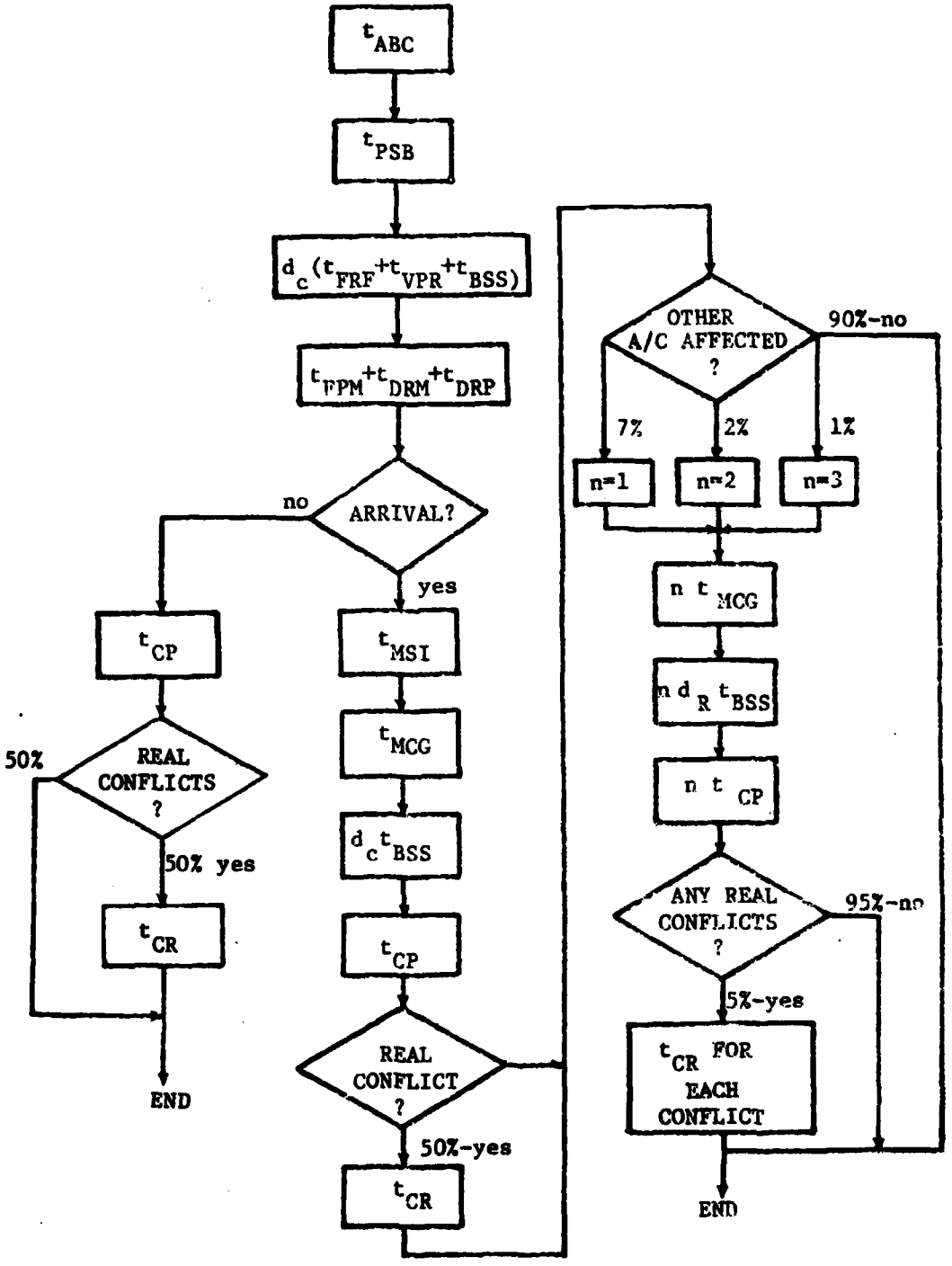

FIGURE 2-3
REQUIRED PROCESSING TIME FOR INITIAL PROCESSING FUNCTION

FIGURE 2-4
REQUIRED PROCESSING TIME FOR HANDOFF MANAGEMENT FUNCTION

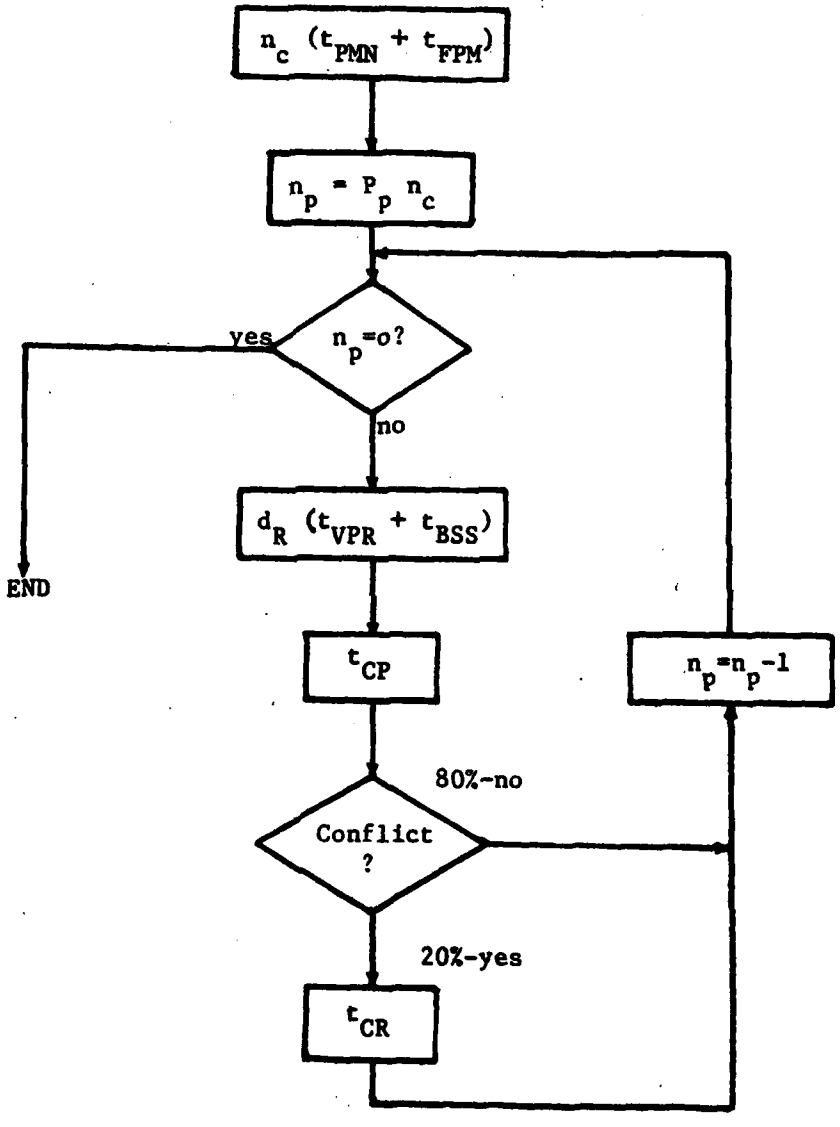

FIGURE 2-5
REQUIRED PROCESSING TIME FOR PROGRESS MONITOR FUNCTION

the control of the center as well as all aircraft that have had initial processing performed (i.e., in-bounds). Based on this progress deviation check, the number of aircraft that deviate sufficiently enough that the vertical profile and state segments must be recomputed (n_p) is determined. For each of these aircraft, processing time is determined for the rebuilding of the vertical profile and state segments for the remaining distance through the center (d_R). Processing time required to invoke conflict prediction and, if necessary, resolution is then determined.

2.1.2.4 Clearance Delivery Function

The clearance delivery function is invoked each time that AERA sends a clearance to an aircraft. The function is defined in Figure 2-6. Four tasks are required for clearance delivery: formulation and delivery of the clearance, updating of the flight plan billboard, updating of the clearance list, and recording of the clearance.

2.1.2.5 Periodic Update Function

The periodic update function, which is described in Figure 2-7, updates pertinent flight information for each individual aircraft at five minute intervals beginning after the completion of initial processing. If an aircraft deviated such that the progress monitor function was required to rebuild the vertical profile and the state segment, updating then occurs at five minute intervals beginning with the time that the last progress monitor function completed.

If the specific aircraft is an arrival, the function begins by examining the arrival's metering progress and issuing metering commands, if appropriate (t_{MCG}). Conflict prediction and, if necessary, resolution are then invoked. In previous requirements for conflict predict, the prediction was made for the period of the present time through twenty minutes into the future. However, in the case of the periodic update function, the prediction algorithm is taking the previous prediction results and extending them an additional five minutes into the future. The net result is that each aircraft always has a minimum of fifteen minutes of prediction and not more than twenty minutes.

2.1.2.6 Overhead Function

There are several tasks that are invoked by the system at specified intervals. For this modeling effort, these tasks have been lumped together as an overhead function invoked every ten seconds. The function, defined in Figure 2-8, involves tasks for displays, interfaces, and data recording.

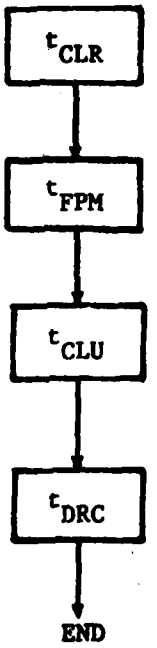

FIGURE 2-6
REQUIRED PROCESSING TIME FOR CLEARANCE DELIVERY FUNCTION

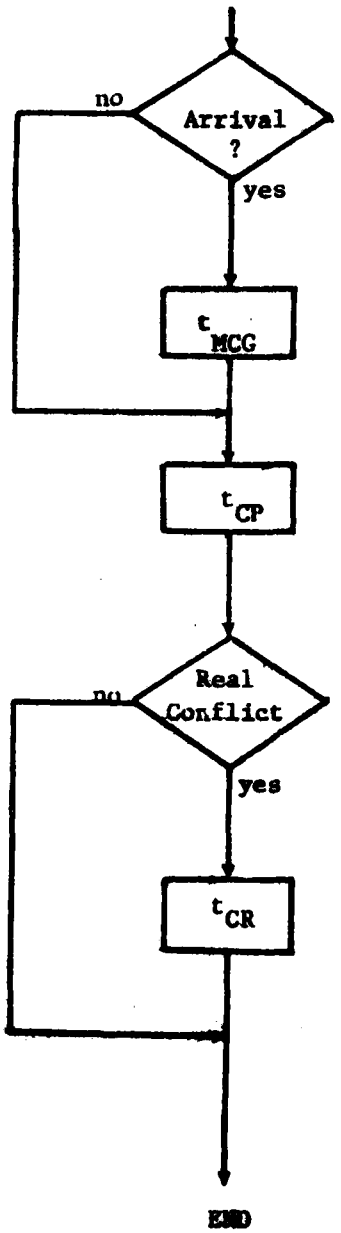

FIGURE 2-7
REQUIRED PROCESSING TIME FOR PERIODIC UPDATE FUNCTION

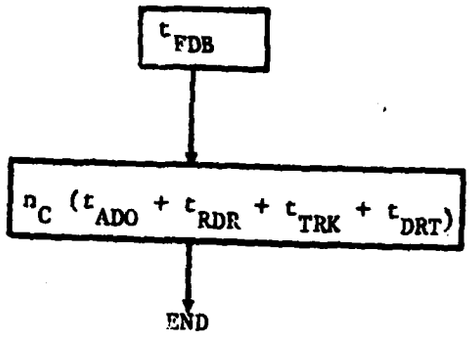

FIGURE 2-8
REQUIRED PROCESSING TIME FOR OVERHEAD FUNCTION

2.1.2.7 Wind Update Function

The wind update function, as defined in Figure 2-9, updates wind estimates every fifteen minutes.

2.1.2.8 Conflict Prediction Task

As previously mentioned, conflict prediction and conflict resolution are invoked by other AERA functions. However, since they are rather complex, prediction and resolution are also defined algorithmically.

Figure 2-10 presents the definition of conflict prediction. The function begins with a term required to set up the prediction data (t_{CTO}). After the data is initially set up, certain aircraft are subjected to a gross filter (t_{CGF}) and a final filter (t_{CCT}). The number of aircraft submitted to the gross filter is a function of the number of aircraft in the center (n_C), a typical fraction of active aircraft given to the gross filter, and the relative route length (d_c/d_t). The number of aircraft submitted to the final filter is a function of the nubmer of aircraft given to the gross filter and a typical fraction of active aircraft given to the final filter. Additionally, the final filter term is modified by an expression indicative of the number of state segments considered during prediction.

2.1.2.9 Conflict Resolution Task

The conflict resolution function is defined in Figure 2-11. The function begins by requiring time for resolution overhead (t_{CRO}). After initial overhead, it can be determined whether altitude resolution or path resolution is best suited for the specific case of interest. If path resolution is decided upon, then path probe (t_{PPR}) is invoked. If path probe is successful, then the actual path resolution (t_{PRE}) is invoked, alternatively the information gained to this point is saved and the algorithm begins again. Path resolution then continues at the point where altitude resolution begins.*

Altitude resolution begins by invoking the vertical profile builder. If altitude resolution appears to be successful at this point, then the state segments are built, otherwise, the algorithm begins again. At this point the resolution algorithm is reasonably sure of a success, therefore, the resolution plan is submitted to the conflict prediction algorithm to ensure that no conflicts still exist. If

* The assumed processor times for path probe and path resolution are very conservative and reflect the early state of processor development.

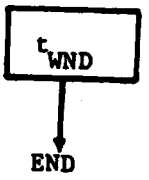

FIGURE 2-9
REQUIRED PROCESSING TIME FOR WIND UPDATE FUNCTION

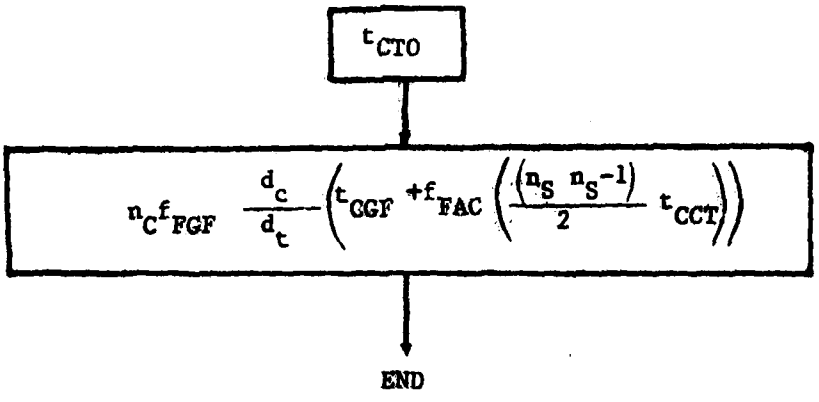

FIGURE 2-10
REQUIRED PROCESSING TIME FOR CONFLICT PREDICTION TASK

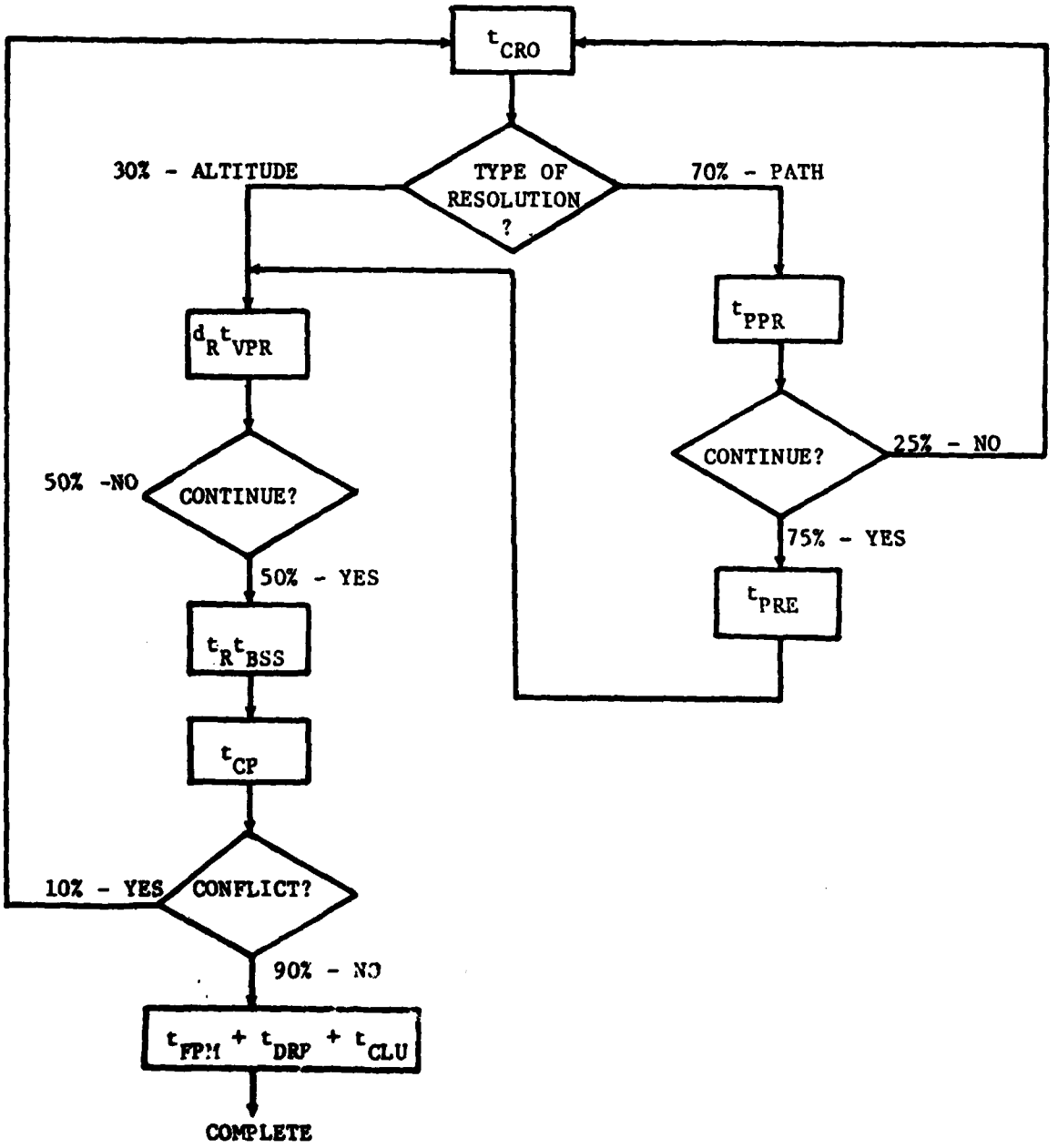

FIGURE 2-11
REQUIRED PROCESSING TIME FOR CONFLICT RESOLUTION TASK

there are still conflicts, the resolution algorithm begins again, otherwise it updates displays, records data and is completed. It should be noted that for the algorithm defined, a significant amount of looping could occur. In the GPSS model of this algoritm, resolution can begin over again only once. The model was implemented this way due to a lack of data with regards to how the decision probabilities change during the course of the resolution algorithm.

2.1.3 Processor Simulator

Once the functions are defined, they are queued at the processor for service. The processor simulator is responsible for the simulation of processor system and its interaction with the defined functions. The simulated processor system may range from a single large CPU to a system of distributed small processors.

Since the actual replacement processor that AERA will eventually be run on was unknown at the time of the analysis, no specific processor was simulated. Rather, during each simulated ten second cycle, the amount of processor capability required to process all functions in the queue at that time was determined. The determined amount of processor capability was made available every ten seconds, thus allowing all of the functions in the queue to be processed. Although this procedure does not address the question of response time, since a function waits no more than ten seconds for service, it does allow for an estimation of the amount of processor capability required during each ten second period.

2.2 Required Memory Model

A linear model to determine the number of bytes of memory required by AERA is now presented. The model relates the amount of memory to requirements for fixed overhead tables as well as to requirements for dynamic data (e.g., aircraft related data). The expression for required memory for a complete center is;

$$M_{KBYTES} = M_{TS} + M_{FT} + M_E n_s + M_{AC}(n_{IAC} + n_{IN})$$

Where:

M_{KBYTES} = Requred Memory in thousands of bytes

M_{TS} = Memory Required for Task Space

M_{FT} = Memory Required for Fixed Table Space

M_E = Memory Required Environmental Data Space per Sector

n_s = Number of Sectors in the Center

M_{AC} = Memory Space Required per Aircraft

n_{IAC} = Number of Instantaneous Aircraft

n_{IN} = Number of Inbound Aircraft

The model makes no assumption with regard to the ratio of buffered to non-buffered memory.

3. RESULTS

This section presents the results of the application of the described models to the 9020 replacement problem. The first part of this section enumerates the environmental data used by the model. The environment data description is followed by a presentation the actual results of the analysis.

As indicated in Section 2, the functional level model requires certain environmental data that characterizes a particular ARTCC. Due to the availability of data, the Washington Center was selected as the source of all required environmental data.

Table 3-1 shows the aircraft related data representative of the Washington Center. Shown for each traffic classification is the percentage of the total traffic and the average time that an aircraft spends under the control of the center. It should be noted that the Washington Center overflights are primarily north-south traffic from or to New York. The arrivals which receive metering service are primarily flights bound for Baltimore-Washington International, National, and Dulles Airports.

Figure 3-1 presents the average processor utilization per ten second period imposed by the modeled AERA functional load for a range of instantaneous aircraft counts (IACS). The processor utilization is specified in terms of 9020A and PDP 11/70 seconds per second. (The 9020A and PDP 11/70 are representative of computer technologies from the mid-sixties and mid-seventies, respectively. The PDP 11/70 is also being used to develop a test bed model of the AERA system.) For the curve shown in Figure 3-1, the model was exercised for three values of IAC (e.g., 100, 250, 400) as indicated. It is emphasized that the results presented in Figure 3-1 are only average processor utilizations, and do not address the issues of response time and peak utilization. From these results, it is clear that AERA will impose significantly larger processor requirements than the existing NAS, which is certainly not requiring more than three 9020A seconds per second for IACS less than 250.

Figure 3-2 presents the distribution of the processing time, measured in PDP 11/70 seconds, required to process all AERA functions queued for service at the end of every ten second period. These distribution curves, which show the percent of the total ten second periods that require specified levels of required processing times, indicate a considerable range of required processing times when all periods are examined. The distribution plots are presented to emphasize the variability of amount of required processing time.

TABLE 3-1
AIRCRAFT RELATED DATA

TRAFFIC CLASSIFICATION	PERCENT OF TOTAL TRAFFIC	AVERAGE TIME UNDER CENTER CONTROL (MINUTES)
OVERFLIGHTS	51%	34
ARRIVALS	34%	26
INTRA-CENTER	15%	60

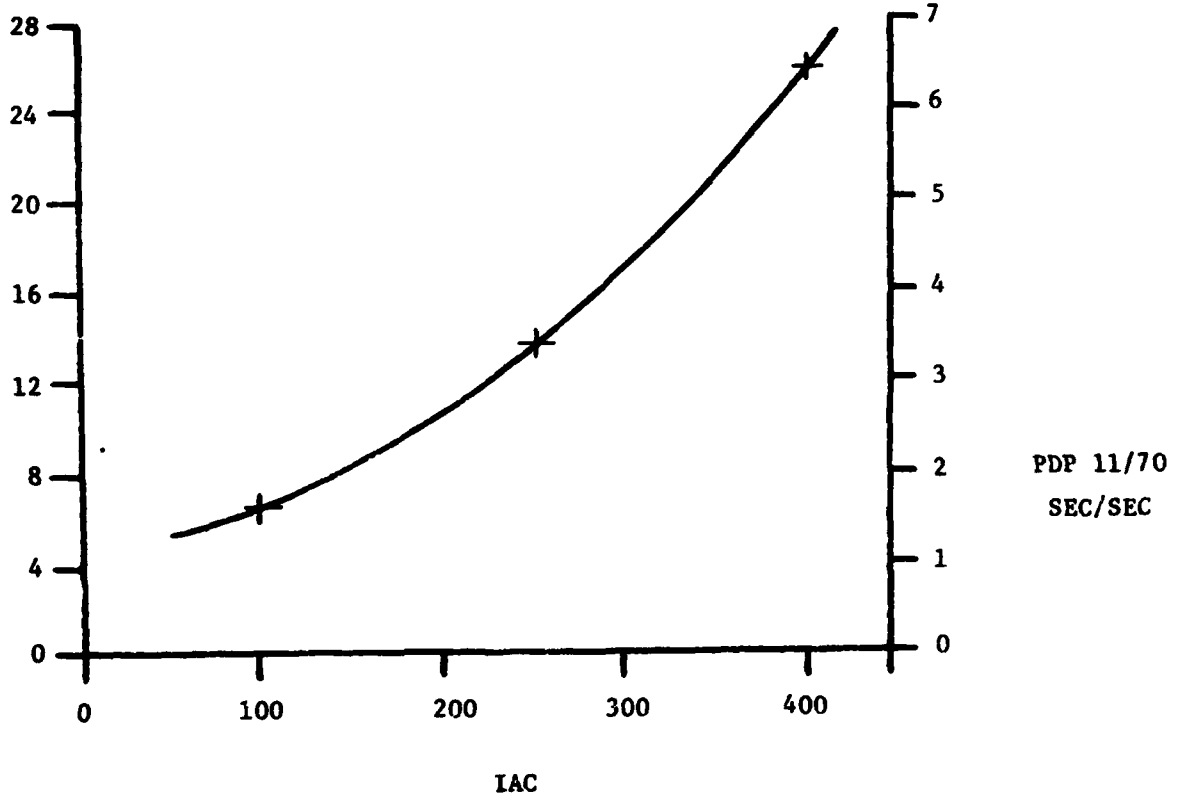

FIGURE 3-1
AVERAGE UTILIZATION OF TEN SECOND PERIOD
DUE TO AN AERA IMPOSED LOAD

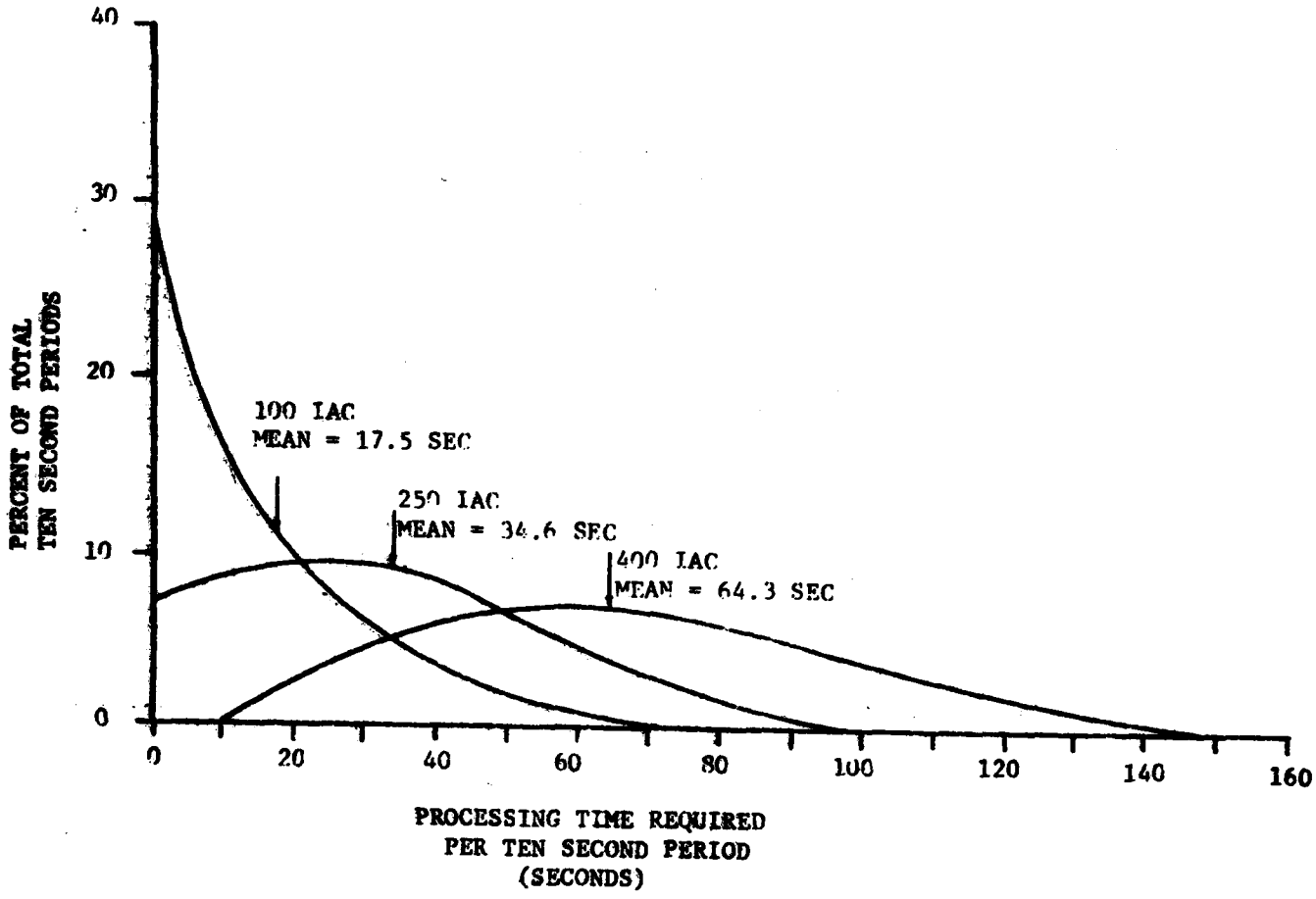

FIGURE 3-2
DISTRIBUTION OF PROCESSING TIME REQUIRED PER TEN SECOND REAL TIME CYCLE
(ASSUMES PDP 11/70)

Figure 3-3 presents the results of applying the described memory model to the Washington Center environment and to an IAC range equal to that of the processor loading analysis. The memory analysis assumes a fixed table space of 20K bytes, an environmental data space per sector of 30K bytes, and 38 sectors in the center. The dashed horizontal line indicates the required memory due to the fixed tables and the sector environmental data. The other two lines represent a nominal estimate and upper bound on the amount of required memory. The nominal estimate assumed that each aircraft requires 4K bytes and that the required task space is 300k bytes. The upper bound assumes an individual aircraft requirement of 8K bytes and a task space requirement of 1000K bytes.

The presented estimates of required memory are extremely conservative for three reasons. First, the environmental data was sized for the fairly complicated route structures of a low altitude sector. This was multiplied by the total number of sectors in the center even though many sectors will essentially share the same data (e.g., high altitude and overlying superhigh sectors). Second, the individual aircraft storage reserved is large and represents construction of rather complicated flight profiles for all aircraft. The 8K byte upper estimate represents an implementation limit of the AERA testbed. Third, the task space assumed that basically all of the code, which represents a significant level of complexity, is resident in main memory. It should be noted that while the memory estimates are large, modern memory systems are able to accommodate the AERA function.

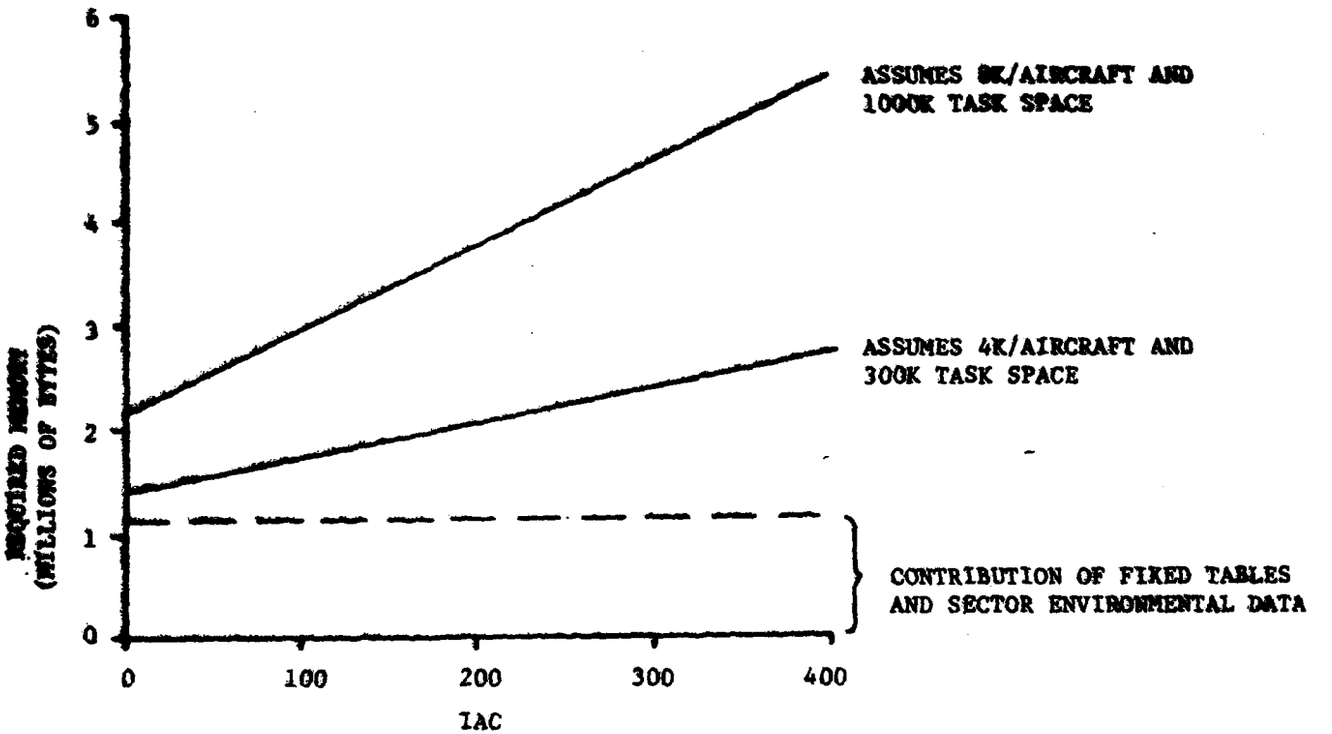

FIGURE 3-3
ESTIMATED MEMORY REQUIRED

APPENDIX A

NOTATION

A1. INTRODUCTION

This appendix provides a definition of the notation used throughout this report. The enumeration of terms is presented in two sections: processing time terms and miscellaneous terms. The processing time terms specify the tasks, with known deterministic processing time, that comprise the AERA functions. The miscellaneous terms specify the required variables used in the models.

A2. PROCESSING TIME TERMS

A list of the processing time terms follows. The list includes a definition of the term and the estimated value of the term in PDP 11/70 milliseconds. The source of the term values is the AERA testbed development effort. In some case, the values of the terms have been roughly measured from execution of existing software code. The measurements were obtained from the AERA simulation software running on the MITRE IBM 370-148. The timing estimates were then converted to PDP 11/70 execution times using an IBM 370/148: PDP 11/70 execution time ratio of approximately 1:1 as determined by A. Macker (MITRE Memorandum W46-M0592, October 20, 1977). In cases where software is not existing, engineering estimates have been made of the values.

TERM	DEFINITION	VALUE (11/70 ms)
t_{ABC}	Time required for overhead in absorbing flight plan and setting up aircraft bead	20
t_{ADO}	Time required for automatic data block offset per aircraft	0.3
t_{BSS}	Time required to process state segments given altitude and speed commands exist for a unit length* route	1
t_{CCT}	Time required for final conflict test	5
t_{CGF}	Time required for gross conflict filter	2
t_{CLU}	Time required to update clearance list	3
t_{CCR}	Time required to formulate and deliver clearance	10
t_{CP}	Time required for conflict prediction task	determined dynamically
t_{CR}	Time required for conflict resolution task	determined dynamically
t_{CRO}	Time required for resolution overhead	300
t_{CTO}	Time required for conflict test overhead	90
t_{DRC}	Time required for record delivered clearance	0.5
t_{DRM}	Time required for miscellaneous recording	0.3
t_{DRP}	Time required to record a profile	3
t_{DRT}	Time required to record track data	0.2

*unit length = one mile

TERM	DEFINITION	VALUE (11/70 ms)
t_{FDB}	Time required to prepare full data block	7.5
t_{FPM}	Time required for one update of the flight plan billboard	3
t_{FRF}	Time required to process one unit length flight plan test to aircraft route segments	33
t_{HOF}	Time required for handoff management	10
t_{MCG}	Time required to generate metering command	500
t_{MSI}	Time required to insert one aircraft into metering schedule	100
t_{PMN}	Time required for progress deviation check	0.125
t_{PPR}	Time required for path probe	2000
t_{PRE}	Time required for path resolution	8000
t_{PSB}	Time required to process prior sector data	100
t_{RTR}	Time required per target to prepare radar message	0.2
t_{TRK}	Time required to absorb NAS track and and store AERA track	2
t_{VPR}	Time required to process vertical profile for a unit length flight	1
t_{WND}	Time required to process wind update	100

A.2 Miscellaneous Terms

TERM	DEFINITION
d_C	Distance of flight through center
d_R	Flight distance from present position through remainder of center
d_T	Sum of all center airway distances
f_{FAC}	Fraction of aircraft reaching final conflict test
f_{FGC}	Fraction of aircraft reaching gross conflict filter
n_c	Number of active aircraft
n_p	Number of deviated aircraft
n_s	Number of state segments coaidered during conflict test per aircraft
P_p	Percentage of active aircraft that typically have deviated
n_{IN}	Number of inbound aircraft